REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 12-17 and 23-36 are pending. Claims 23-36 have been objected to. Claims 12-17 have been rejected.

Claims 1 and have been amended. No claims have been canceled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicant submits that the amendments do not add new matter.

OBJECTIONS TO THE CLAIMS

Examiner objects to claims 23-36 and asserts that there is insufficient antecedent basis for "a bit line formed in the slot" limitation in the claims, that "the slot" is not defined prior to the last paragraph of claim 30.

Applicant has amended claim 30 in light of the Examiner's objection.

Applicant respectfully submits that claims 23-36 are now allowable.

REJECTIONS UNDER 35 U.S.C. § 112

Claims 12-17 have been rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Examiner asserts that the claims contain subject matter not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The Examiner stated that "None of the drawings and the specifications disclose a single one dimensional slot that has an access to plurality of active regions. Furthermore, a bit line cannot be formed in a single one-dimensional slot. By definition, to be able to form in any entity, the entity needs to have more than one-dimension. Having a substantially larger length than a width, does not make something one-dimensional."(Office Action, 03/07/07, p.2).

Applicant has amended claim 12 to remove the word "single" from claim 1 in light of the Examiner' s rejection.

Applicant has amended claim 12 to include a one-dimensional slot patterned in the ILD, wherein the one dimensional slot is to provide access to the plurality of active regions; and a bit line formed in single slot, wherein the bit line is to contact the plurality of active regions through the slot, wherein the one-dimensional slot has a length along the length of the bit line that is substantially larger than a width that is the gate stack width.

Applicant respectfully submits that the discussed limitations, as recited in amended claim 12, are supported by the Specification, drawings, and claims, as originally filed. Applicant respectfully submits that the "one dimensional slot" is clearly defined in the Specification and does not mean the length without any width.

More specifically, the Specification discloses:

> In block 428, a layer of resist 528 is deposited over the array 400. FIGS. 5K, 5L, and 5M display the resist layer 528 from different angles. FIGS. 5K and 5L illustrate the patterned resist layer 528 using cross sectional views, while FIG. 5M illustrates the patterned resist layer using an overhead view. FIG. 5L shows a view along the line C 316 in FIG. 3A. As can be seen, the gate stacks 518a, 518e, and 518f align along separate bit lines 302a, 302b, and 302c respectively. The resist 528 may be deposited using photolithography as described above, and is patterned to protect the areas of the ILD 526 that are to remain, while exposing those that should be removed. The ILD 526 should be removed in the area above the gate stacks 518. As can be seen, the resist layer 528 has a slot pattern in it. A slot is a one-dimensional image, which can be printed much easier and smaller than a two-dimensional image. The slot pattern has a length along the bit line that is much greater than its width, which will be approximately the gate width. For example, the bit line may be 200 .mu.m long while the gate is 100 nm wide, so the slot would be 200,000 times longer than it is wide.

(Specification, paragraph [0030], **Figure 5M**) (emphasis added)

As clearly shown in **Figure 5M**, two slot patterns are formed between three portions of resist 528. As shown in **Figure 5M**, one of two slot patterns runs over gate stacks 518a-518d with active region 524a-524c. As shown in **Figure 5M**, another of two slot patterns runs over

gate stacks 518e-518i with active regions 524d-524e. As shown in **Figure 5M**, each of the two slot patterns [singular] provides an access to the plurality of active regions.

Figure 5N and paragraph [0036] disclose an etched ILD layer so that a slot [singular] is formed along gate stacks 518a and 518c with active regions 524a-524c [plural]. As shown in **Figure 5N** the slot [singular] provides access to the plurality of active regions, as recited in amended claim 12.

Figure 5O and paragraph [0037] disclose a deposited conductive plug into the slot [singular] that forms a bit line that contacts the plurality of active regions 524a-524c though this slot [singular], as recited in amended claim 1.

Therefore, applicant respectfully submits that amended claim 1 is patentable under 35 U.S.C. § 112, first paragraph.

Given that claims 13-17 depend from amended claim 12, and add additional limitations, applicant respectfully submit that claims 13-17 are patentable under 35 U.S.C. § 112, first paragraph.

CONCLUSION

In view of the foregoing, Applicant respectfully submits the present application is now in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned at (408) 720-8300.

If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 04/19/2007 By: _____

Tatiana Rossin
Reg. No. 56,833

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(408) 720-8300
Fax (408) 720-8383